Introduction

About PCM
- Multi-level cell (MLC) PCM offers high density with low per-byte fabrication cost.
- The energy for programming intermediate states is considerably larger (10 times) than programing single-level cell PCM.

Motivation for Restricted-Coset Coding
- When the encoding granularity decreases, the data symbol energy decreases.
- The auxiliary symbol energy gradually increases and reaches its maximum at the granularity of 8-bits.
- Our goal is to take advantage of fine-grain encoding granularity while reducing the overhead of auxiliary symbols.
- We introduce a lightweight compression provides enough space in the memory line to store auxiliary symbols.

On-chip WLCRC architecture for 16-bit granularity
- WLCRC compression+coding and decoding+decompression for a data block granularity of 16.
- The 8 64-bit encoders operate in parallel.
- Each encoder splits the word into 16-bit blocks.
- Total encoding space overhead < 0.4%.
- The decoding follows the reverse structure of the encoding.

Word Level Compression (WLC) + Restricted Coset Coding
- The k most significant bits (MSBs) of most 64-bit words have the same binary value and thus can be represented by only one bit.
- For 4MSBs, 5MSBs and 6MSBs, WLC compresses more than 90% of the memory lines.
- (a) Word Level Compression (WLC), (b) Restricted coset coding at 16-bit granularity.

Experimental Settings
- To conduct experimental tests, a trace driven simulator is developed. The input traces to our simulator are collected with Virtutech Simics.
- WLCRC-16 does not change the bits in the data except in only a few locations, which allows the differential write to take advantage of data locality.
- WLCRC-16 uses 39% less energy than the leading approach.